

REMARKS

I. Status of the Application

Claims 1-11, 13 and 14 are pending in this application. Claims 16-22 have been withdrawn in accordance with an election referenced in page 3 of the December 3, 2004 office action. In the May 4, 2005 office action, the Examiner:

A. Rejected claims 1-11, 13 and 14 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement;

B. Rejected claims 1-11, 13 and 14 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite; and

C. Rejected claims 1-11, 13 and 14 under 35 U.S.C. § 103(a) as allegedly being obvious over U.S. Patent No. 6,772,512 to Tsai (hereinafter “Tsai”) in view of U.S. Patent No. 4,881,885 to Kovac et al. (hereinafter “Kovac”).

In this response, applicant has amended claims 1-11 and 13-14, and added new claims 23-31. Applicant has further canceled the withdrawn claims 16-22, without prejudice. Applicant respectfully traverses the rejection of claims and requests reconsideration in view of the foregoing amendments and the following remarks.

II. The Inadequate Written Description Rejection is Moot

The Examiner has rejected claims 1-11, 13 and 14 as failing to comply with the written description requirement of 35 U.S.C. §112. In particular, the Examiner objected to the

recitation of a “package” and a “chip mechanically fixed (to the interconnect layer)” in claim

1. (May 4, 2005 office action at p.3).

With regard to the recitation of the package, claim 1 has been amended to claim an *arrangement* for use in a package, as opposed to claiming the package itself. The specification clearly conveys to one of ordinary skill in the art that an arrangement having a supporting substrate and a chip attached thereto (within an intervening bonding channel) may conventionally be used in a package. (See Specification as filed at p.1, lines 11-30). The novel arrangement of these elements as described and claimed in the application is clearly intended for such use. (See Specification at p.4, line 33 to p.5, line 9).

Accordingly, the specification clearly conveys to one of ordinary skilled in the art that the combination of elements of claim 1 are usable in a package.

With regard to the “chip mechanically fixed” language, the claim 1 has been amended to recite that the chip is “fixed” without the limitation “mechanically”. The specification and drawings plainly disclose examples of a chip that is fixed to the interconnect layer. For example, Figs. 1A, 2A, 3A, 4A and 5A all show the chip 112 fixed to the interconnect layer 110. In addition, the description at page 11, lines 15-17, reads, “the chip 112 may be applied on the outer surface 110a of the interconnect layer 110 by the bilaterally adhesive material”.

Accordingly, the specification clearly describes examples of arrangements in which a chip is fixed to an interconnect layer in accordance with claim 1.

In view of the foregoing amendments and remarks, it is respectfully submitted that the rejections under 35 U.S.C. §112, first paragraph are moot and should be withdrawn.

**III. The Indefiniteness Rejection of Claims 1-11, 13 and 14 is in Error**

The Examiner has rejected claims 1-11, 13 and 14 as being indefinite. In particular, the Examiner objected to the claim recitation of “mechanically fixed” because, according to the Examiner, it is “not clear what is included /excluded by the expression “mechanically fixed”. (May 4, 2005 office action at p.4). As discussed above, the term “mechanically” has been canceled from the claims. It is respectfully submitted that one of ordinary skill in the art would understand the scope of the term “fixed” as used in claim 1, given the ordinary meaning of that term. Accordingly, it is respectfully submitted that the indefiniteness rejection of claims 1-11, 13 and 14 should be withdrawn.

**IV. Claim 1 is Patentable Over Tsai and Kovac**

In the May 4, 2005 office action, the Examiner rejected claim 1 as being allegedly being obvious over Tsai in view of Kovac. For reasons discussed below in detail, there is no motivation or suggestion to modify Tsai with the “escape prevention structure” of Kovac. It is therefore respectfully submitted that the obviousness rejection of claim 1 should be withdrawn.

**A. The Present Invention**

Claim 1 is directed to an arrangement for use in a package that includes a supporting substrate, an interconnect layer, a chip, an encapsulation material, and an escape prevention structure. The supporting substrate has a bond opening therein. The interconnect layer is disposed on the supporting substrate and includes a bonding channel that overlaps with the

bond opening. The chip is mechanically fixed to the interconnect layer to cover the bonding channel. The encapsulation material is arranged in the bonding channel. The escape prevention structure enables escaping of air from the bonding channel and substantially prevents the encapsulation material from escaping from the bonding channel.

B. Tsai

Tsai teaches a method of fabricating a flip chip ball grid array package without causing mold flash. The package includes a substrate 210, a chip 220 connected to the substrate using a ball grid array 221, and contact pads 230. The contact pads 230 extend from the side of the substrate opposite the side to which the chip 220 is attached. (See e.g. Tsai at Fig. 2D). The package is encapsulated, except for the contact pads 230. To this end, the package is placed in a specially designed molding fixture. The encapsulation material is passed above and below the chip 220 and freely flows on both sides of the chip and then finally out through a hole 211 in the substrate. On the opposite side of the substrate, further lateral flow is impeded by false contact pads 231. (*Id.* and accompanying text).

B. Kovac

Kovac relates to an apparatus that encapsulates a surface and leads of a chip. The apparatus includes a fixture for holding the chip. The fixture includes a recessed well 14 into which the chip 24 is placed. The chip 24 is held within the well by a vacuum applied to the backside of the chip. The Kovac apparatus includes conduits 20 that restrict the overflow of the coating material as a consequence of a combination of factors. The three factors include

the rapid removal of solvent from the coating, the rapid formation of skin of crosslinked material, and a momentum balance between the coating deposition rate and air flow. The finished product of Kovac is removed from the fixture, and is illustrated in Fig. 5.

**C. No Motivation or Suggestion to Modify  
Has Been Set Forth in the Office Action**

In the May 4, 2005 office action, the Examiner appears to have admitted that Tsai does not teach the claimed escape prevention structure because the Examiner relies on the teachings of Kovac for that element. (May 4, 2005 office action at p.5). However, the Examiner has not set forth any motivation or suggestion to modify Tsai with teachings of Kovac. (*Id.*) An obviousness rejection cannot be based on a mere combination of references. There must be a legally sufficient motivation or suggestion to combine teachings of different references. Because there does not appear to be any motivation or suggestion to make the combination proposed by the Examiner, it is respectfully submitted that the obviousness rejection of claim 1 is in error and should be withdrawn.

**D. One of Ordinary Skill in the Art  
Would Not Modify Tsai as Proposed**

There is no reason one of ordinary skill in the art would modify Tsai to place escape prevention structures in a bonding channel as claimed. Tsai has a different structure, and requires a different encapsulation arrangement that would be defeated if the claimed escape prevention structures were employed.

In particular, as alleged by the Examiner, the interconnect layer of Tsai is the ball grid

array 221, and the bond opening is the hole 221 (i.e. “p”) in the substrate 210 (*Id.* at p.5; Tsai at Figs. 2A and 2D). As claimed, the “bonding channel” is in the interconnect layer and overlaps with the bond opening. The only possible “bonding channel” of Tsai is the area between and among the ball grid array 221 between the chip 220 and the substrate 210, which also overlaps the hole 211.

As clearly shown in Figs. 2D and 2F, the encapsulation material is *clearly intended* to flow out of the “bonding channel” of Tsai. Instead of preventing escape, the encapsulation material is intended to flow both *above* the chip 220, and partially *below* the substrate 210, and clearly *laterally outside* the “bonding channel”. Thus, any attempt to place an escape prevention structure to prevent encapsulation material from exiting the bonding channel would inhibit the desired flow of material *around* the chip outside of the “bonding channel” of Tsai.

One of ordinary skill in the art would not modify Tsai to substantially prevent encapsulation material from flowing outside of a bonding channel that is located in its ball grid array “layer” because it would defeat the purpose of Tsai to encapsulate the entire chip, including portions external to the ball grid array. For at least this reason, it is respectfully submitted that the obviousness rejection of claim 1 should be withdrawn.

E. Conclusion as to Claim 1

For the multiple independent reasons discussed above, as well as others, it is respectfully submitted that the obviousness rejection of claim 1 over Tsai and Kovac is in error and should be withdrawn.

V. Claims 2-11, 13 and 14

Claims 2-11, 13 and 14 also stand rejected as allegedly being obvious over Tsai in view of Kovac. Claims 2-11, 13 and 14 depend from and incorporate all of the limitations of claim 1. Accordingly, for at least the same reasons as those set forth above in connection with claim 1, it is respectfully submitted that the rejection of claims 2-11, 13 and 14 over Tsai and Kovac should be withdrawn.

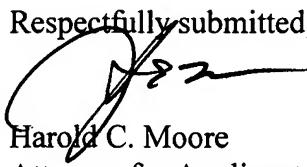
VI. New Claims 23-31

New claims 23-31 are allowable over the prior art of record for reasons similar to those discussed above in connection with claim 1.

VII. Conclusion

For all of the foregoing reasons, it is respectfully submitted the applicants have made a patentable contribution to the art. Favorable reconsideration and allowance of this application is, therefore, respectfully requested.

Respectfully submitted,

  
Harold C. Moore  
Attorney for Applicants  
Attorney Registration No. 37,892  
Maginot Moore & Beck  
Bank One Center Tower  
111 Monument Circle, Suite 3000  
Indianapolis, Indiana 46204-5115  
Telephone: (317) 638-2922